

REMARKS/ARGUMENTS

Claims 1-21 are indicated as pending in this application. It appears that page 10 of this application comprising claims 22-28 may have been missing. Accordingly, claims 22-28 are presented herein. Claim 22 has been cancelled, as it is now incorporated in amended claim 21.

The Examiner has objected to the specification. In particular, the Examiner states that in claim 4, the limitation “the input trigger circuit is non-responsive to a pulse duration of said pulse input signal” does not find support in the specification.

If the Examiner will turn to page 5 of the specification, he will see that the specification states in paragraph 0013 at lines 10-11 “the duty cycle of the single timed output pulse is irrelevant, further simplifying the control provided by the microcontroller”. What this means is that the pulse width or duty cycle of the single timed output pulse from the microcontroller is irrelevant. In the embodiment shown, the circuit is edge triggered, in particular, rising edge triggered, so the pulse width of the control signal from the microprocessor is irrelevant, i.e., the circuit is non-responsive to pulse width, as claimed. This is shown also graphically in Fig. 4 which shows that the high and low output signals HO and LO respectively, are determined by the triggering input signal TRIG, and in particular, the rising edge of TRIG determines when the LO signal goes low and after the dead time DT, when the HO signal goes high. The width of the pulses of signal TRIG is irrelevant. Accordingly, it is submitted that the specification adequately describes what is claimed in claim 4. Further, as an original claim, claim 4 is part of the original specification.

The Examiner has also objected to the drawings. A new drawing Fig. 1 clearly showing the pulse input signal, the input trigger circuit and the shut down circuit is included herewith. The pulse input signal is the input to the input TRIG provided by the microcontroller. The input trigger circuit includes circuit elements 140, 220, the gates that are not numbered and can include the level shift circuit 180. This circuit drives the drivers 190 and 200. The input trigger circuit can also include the dead time circuit 170.

The shutdown circuit includes the circuit element 150 and its connection to the two gates in the input trigger circuit, which are illustratively shown as AND gates. When the circuit

element 150 produces a low level signal, the two AND gates are disabled, thereby disabling the drivers.

Claim 8 has been amended to address the claim 8 objection.

Turning to the rejection of the claims, the Examiner has rejected claims 1-5, 7-14 and 16-18 under 35 U.S.C. §102 as being anticipated by Liu et al., U.S. Patent No. 5,598,326. The Examiner further rejects claims 6 and 15 under 35 U.S.C. §103 as being unpatentable over Liu in view of Takahara et al., U.S. Patent No. 6,031,726.

Claim 1 and the other independent claims have been amended to recite that when the first and second drive circuits provide the first and second drive signals, the input trigger circuit is nonresponsive to the pulse duration of the pulsed input signal. As described above, the input trigger circuit of the present invention is nonresponsive to a pulse duration of the pulsed input signal. In the illustrated embodiment, the input trigger circuit is responsive to the rising edge but is not responsive to the pulse duration of the pulsed input signal. This allows for very simple control by a microcontroller.

In U.S. Patent No. 5,598,326 to Liu, and in particular, in Fig. 4, the trigger circuit used there is responsive to the pulse width. In particular, the DV/DT circuit 28 produces the signal E shown in Fig. 5 from the pulse train C produced by the voltage comparator 26. As the Examiner can appreciate, the circuit 28 is positive and negative triggered, that is, it is triggered by the pulse train C on both the positive and negative edges of the pulse train. As a result, it is responsive to the pulse width or duty cycle of the pulse train C. The Examiner asserts that the flip flop 50, however, of the voltage and current limiting circuit produces a disable signal to the gates 30 and 31 to disable these gates, thereby making the circuit nonresponsive to a pulse duration of the pulsed input signal C. However, when this is the case, there is no output from the circuit either. That is, there are no driver outputs to the transistor Q1 and Q2, as the drivers are shut down by the disabling of the AND gates 30 and 31.

According to the present invention, the circuit is non-responsive to the pulse duration of the pulsed input signal even when driver output signals are provided to the half-bridge switching circuit. Claim 1 now recites “wherein, when the first and second drive circuits provide the first and second drive signals, the input trigger circuit is non-responsive to a pulse duration of the

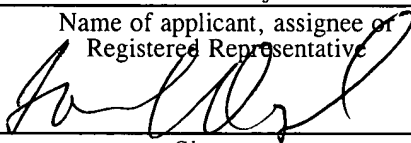
pulsed input signal. The circuit shown in the Liu reference does not operate as claimed. In the circuit of the Liu reference, when the first and second drive circuits provide the first and second drive signals, the input trigger circuit is responsive to the pulse duration of the pulsed input signal C. Liu is only non-responsive to pulse width when the drivers are disabled. It is responsive to pulse width when the drivers are enabled. According to the present invention, when the drivers are enabled, the circuit is non-responsive to triggering pulse width. Accordingly, it is submitted that the Liu reference fails to teach or suggest the invention as now claimed. The Takahara et al. and the other references cited by the Examiner fail to teach or suggest the invention when combined with Liu.

Accordingly, in view of the above, it is submitted that all claims in this application are now in condition for allowance, prompt notification of which is requested.

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Signature

May 26, 2004

Date of Signature

Respectfully submitted,



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Enclosure: Corrected Drawings